40Gb/S QSFP+ LR4 Transceiver

P/N: TQSFPP-CC1FAAA

Product Features

- Compliant with IEEE 802.3ba 40G BASE-LR4 standards
- QSFP+ MSA compliant
- Up to 11.2Gb/s data rate per channel
- Maximum power consumption 3.5W
- 4 CWDM lanes MUX/DEMUX design
- Single 3.3V power supply
- 0°C to 70°C case temperature operating range
- LC duplex connector
- Up to 10km reach over standard single mode fiber
- I2C management interface
- RoHS-6 Compliant

Application

- Ethernet for 40GBASE-LR4
- InfiniBand DDR & QDR
- Client-side 40G Telecom connections

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Absolute Maximum Rating

Parameter	Min	Max	Unit	Note
Storage Temperature	-40	85	℃	
3.3V Power Supply Voltage	-0.5	3.6	V	
Relative Humidity	0	85	%	
Damage Threshold, each Lane	3.3		dBm	

Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Note
Case Operating Temperature	0		70	℃	
Power Supply Voltage	3.135	3.3	3.465	V	
Date Rate per Channel		10.3125	11.2	Gbps	
Control Input Voltage High	2		Vcc	V	
Control Input Voltage Low	0		0.8	V	
Link Distance with G.652			10	km	

Electrical Characteristics

Parameter	Min	Typical	Max	Unit	Note
Transceiver Electrical Characteristics					
TRx Power Consumption			3.5	W	
Supply Current			1.1	A	
Transceiver Power-on Initialization Time			2000	ms	1
Transmitter (each Lane)					
Single-ended Input Voltage Tolerance (Note 2)	-0.3		4	V	Referred to TP1 signal common
AC Common Mode Input Voltage Tolerance	15			mV	RMS
Differential Input Voltage Swing Threshold	50			mVpp	LOSA Threshold
Differential Input Voltage Swing	190		700	mVpp	
Differential Input Impedance	90	100	110	Ohm	

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Differential Input Return Loss	See IEEE 802.3ba 86A.4.11			dB	10MHz-11.1GHz
J2 Jitter Tolerance	0.17			UI	
J9 Jitter Tolerance	0.29			UI	
Data Dependent Pulse Width Shrinkage (DDPWS) Tolerance	0.07			UI	
Eye Mask Coordinates {X1,X2,Y1,Y2}	{0.11,0.31,95,350}			UI mV	Hit Ratio= $5x10^{-5}$
Receiver (each Lane)					
Single-ended Output Voltage	-0.3		4.0	V	Referred to signal common
AC Common Mode Output Voltage			7.5	mV	RMS
Differential Output Voltage Swing	300		850	mVpp	
Differential Output Impedance	90	100	110	Ohm	
Termination Mismatch at 1MHz			5	%	
Differential Output Return Loss	See IEEE 802.3ba 86A.4.2.1			dB	10MHz-11.1GHz
Common Mode Output Return Loss	See IEEE 802.3ba 86A.4.2.2			dB	10MHz-11.1GHz
Output Transition Time	28			ps	20% to 80%
J2 Jitter Output			0.42	UI	
J9 Jitter Output			0.65	UI	
Eye Mask Coordinates {X1,X2,Y1,Y2}	{0.29,0.5,150,425}			UI mV	Hit Ratio= $5x10^{-5}$

Notes

1. Power-on Initialization Time is the time from when the power supply voltages reach and remain above the minimum recommended operating supply voltages to the time when the module is fully functional.
2. The single ended input voltage tolerance is the allowable range of the instantaneous input signals.

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Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Lane Wavelength	L0	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5	nm	
	L2	1304.5	1311	1317.5	nm	
	L3	1324.5	1331	1337.5	nm	
Transmitter Optical Characteristics						
Side Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	PT			8.3	dBm	
Average Launch Optical Power, each lane	LOP	-7		2.3	dBm	
Optical Modulation Amplitude, each lane	OMA	-4		3.5	dBm	1
Difference in Launch Power between any Two Lanes (OMA)	Ptx,diff			6.5	dB	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TPD), each Lane		-4.8			dBm	
TDP, each lane	TDP			2.6	dB	
Average launch power of OFF transmitter, each lane	Poff			-30	dBm	
Extinction Ratio	ER	3.5			dB	
Relative Intensity Noise	RIN			-128	dB/Hz	12dB reflection
Optical Return Loss Tolerance	TOL			20	dB	
Transmitter Reflectance	R_T			-12	dB	
Eye Mask {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				
Average Launch Power OFF Transmitter, each Lane				-30	dBm	
Receiver Optical Characteristics						
Damage Threshold, each Lane	THd	3.3			dBm	2
Average Receive Power, each Lane		-13.7		2.3	dBm	

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Total Average Receive Power				8.3	dBm	
Receive Power (OMA), each Lane				3.5	dBm	
Receiver Sensitivity (OMA), each Lane	SEN			-11.5	dBm	
Stressed Receiver Sensitivity (OMA), each Lane				-9.6	dBm	3
LOS Assert	LosA	-28			dBm	
LOS Deassert	LosD			-15	dBm	
LOS Hysteresis	LosH	0.5			dB	
Receiver Electrical 3dB upper Cutoff Frequency, each Lane	Fc			12.3	GHz	
Conditions of stressed receiver sensitivity test(Note4):						
Vertical Eye Closure Penalty, each Lane			1.9		dB	
Stressed eye J2 Jitter			0.3		UI	
Stressed eye J9 Jitter			0.47		UI	

Notes

1. Even if the TDP < 0.8 dB, the OMA min must exceed the minimum value specified here.
2. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
3. Measured with conformance test signal at receiver input for BER = $1x10^{-12}$
4. Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

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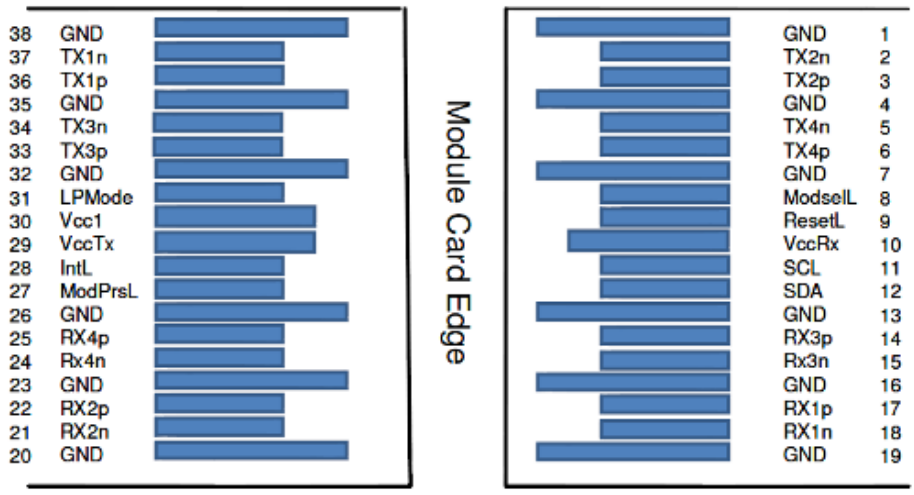
QSFP+ Module Pad Assignments and Descriptions



Top Side
Viewed From Top

Bottom Side
Viewed From Bottom

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	

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19		GND	Ground	1	
20		GND	Ground	1	
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	
30		Vcc1	+3.3V Power supply	2	
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	

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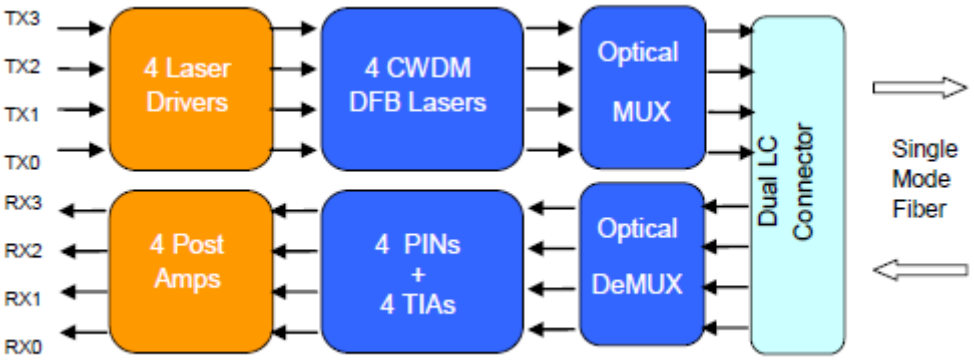
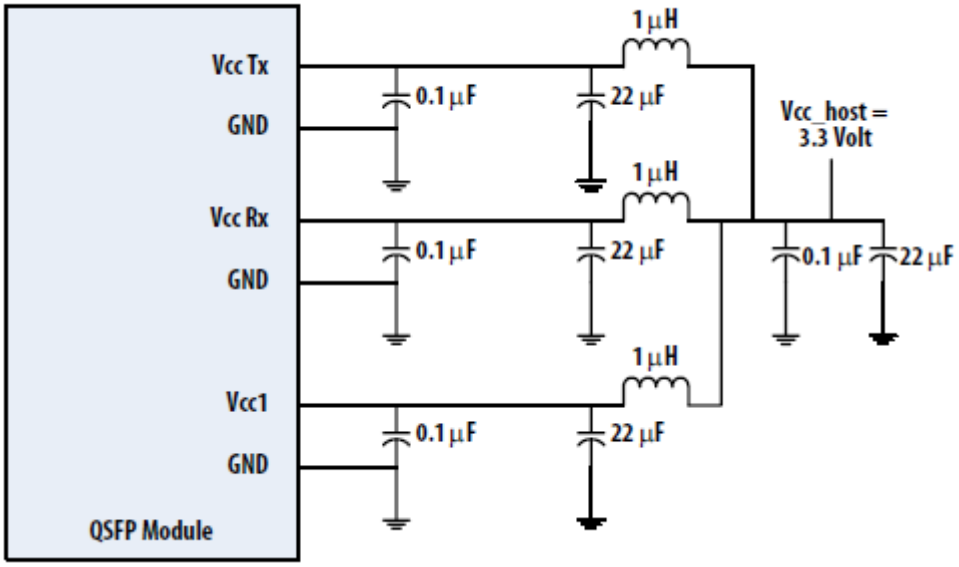
Transceiver Block Diagram



Recommended Host Board Power Supply Circuit



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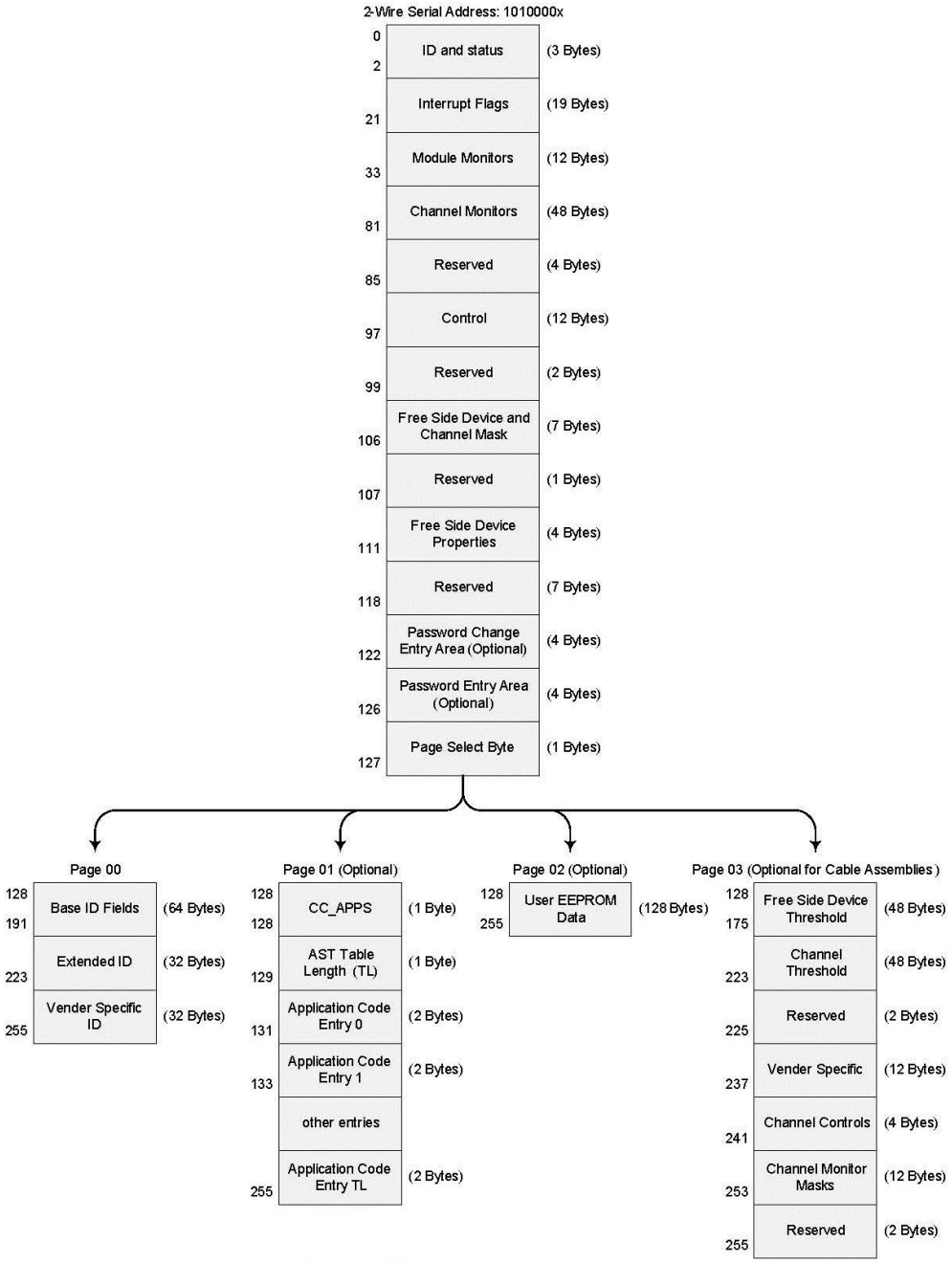
Memory Map

The memory map is structured as a single address and multiple page approaches, according to the QSFP+ SFF-8436 MSA specification as shown in the below. For more detailed description of this memory map or lower pages, please see our Memory Map document with flexible customization settings.



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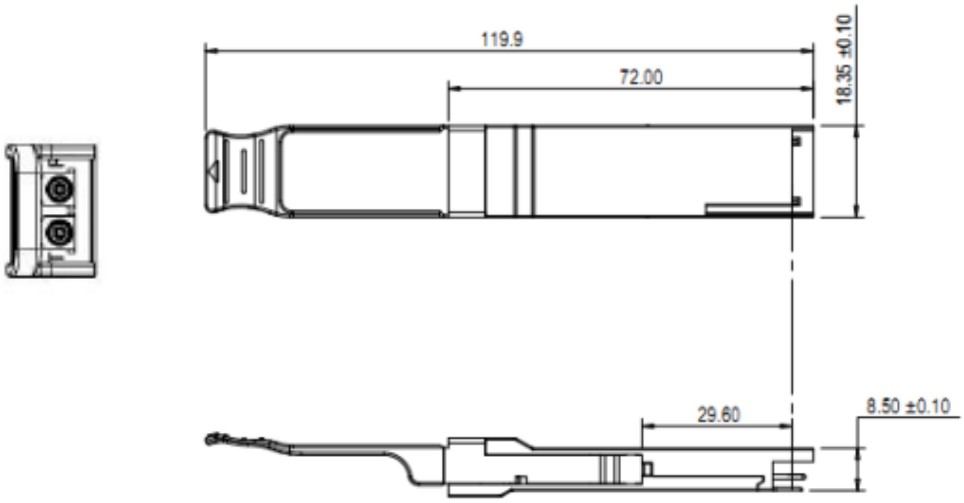
Mechanical Design Diagram

Unit: mm



ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all others electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser Safety

This is a Class 1 Laser Product according to EN 60825-1:2014. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

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